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10/581,395	08/14/2008	Hien Boon Tan	Q78657	3868

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EXAMINER	
GOODWIN, DAVID J	

ART UNIT	PAPER NUMBER
2818	

NOTIFICATION DATE	DELIVERY MODE
03/08/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/581,395	TAN ET AL.	
	Examiner	Art Unit	
	DAVID GOODWIN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-9 and 13-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-9 and 13-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 5, 6, 13, 14, 15, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravorty (US 6181569) in view of Qi (US 6774497).

3. Regarding claim 5.

4. Chakravorty teaches a method of making a device. Said method comprises providing a wafer, the wafer comprising a plurality of integrated circuit chips, and dicing the wafer into a plurality of chip arrays (317) each array comprising two or more integrated circuit chips (fig 9a). Each circuit chip comprises a row of bond pads (311) aligned in a central row (fig 7). Attaching each chip array (317) to a substrate (318) (fig 9b) (column 12 lines 35-55). Dicing each array (317), attached to the substrate(318) into individual chip scale packages, each individual chip scale package (319) comprising only one integrated circuit chip (fig 9e) (column 13 lines 5-25).

5. Chakravortry does not teach the mounting process.

6. Qi teaches a method of making a device. Said method comprises a chip (110) comprising a plurality of bond pads (114) aligned on an upper surface of the integrated circuit chip, wherein each bond of said bond pads is aligned in a row (fig 1). A plurality of conductive bumps (120) formed on the plurality of bond pads (114) (fig 1) (column 4

lines 45-65). Mounting each chip on a substrate (240) such that the bumps align with corresponding solder pad openings (242) on an upper surface of the substrate (240) (fig 2a). Reflowing the chips thereby melting the bumps and establishing a conductive joint between the integrated circuit chips and the substrate (fig 2b). Under fill encapsulating the integrated circuit chip on the substrate (fig 2b) (column 6 lines 1-45).

7. It would have been obvious to one of ordinary skill in the art to form a chip having bond pads so that conductive traces can be connected to the chip.

8. Regarding claim 6.

9. Qi teaches, prior to mounting, dipping each array in flux material such that flux (124) material adheres to the bumps (120) (fig 1). Wherein each array is mounted on a substrate the flux material adheres the bumps to the solder pad openings (242) (fig 2a) (column 5 lines 20-25).

10. Regarding claim 13.

11. Chakravorty teaches prior to mounting each array on a substrate, providing a wafer comprising a plurality of integrated circuit chips (317). Dicing (316) the wafer into of integrated circuit chips comprising two or more integrated circuit chips (9a).

12. Regarding claim 14.

13. Chakravorty teaches a method of mounting a chip scale package. Said method comprises monting an array of integrated circuits (317) on a substrate (318). Each integrated circuit chip (317) comprising a plurality of bond pads (311) on an upper surface of the integrated circuit chip wherein each of said bond pads is aligned in a plurality of central rows (fig 7). A plurality of conductive bumps (314) formed on the

plurality of bond pads (311). Attaching each chip array (317) to a substrate (318) (fig 9b) (column 12 lines 35-55). Dicing each array (317), attached to the substrate(318) into individual chip scale packages, each individual chip scale package (319) comprising only one integrated circuit chip (fig 9e) (column 13 lines 5-25).

14. Chakravortry does not teach the mounting process.

15. Qi teaches a method of making a device. Said method comprises a chip (110) comprising a plurality of bond pads (114) aligned on an upper surface of the integrated circuit chip, wherein each bond of said bond pads is aligned in a row (fig 1). A plurality of conductive bumps (120) formed on the plurality of bond pads (114) (fig 1) (column 4 lines 45-65). Mounting each chip on a substrate (240) such that the bumps align with corresponding solder pad openings (242) on an upper surface of the substrate (240) (fig 2a). Reflowing the chips thereby melting the bumps and establishing a conductive joint between the integrated circuit chips and the substrate (fig 2b). Under fill encapsulating the integrated circuit chip on the substrate (fig 2b) (column 6 lines 1-45).

16. It would have been obvious to one of ordinary skill in the art to form a chip having bond pads so that conductive traces can be connected to the chip.

17. Regarding claim 15.

18. Qi teaches, prior to mounting, dipping each array in flux material such that flux (124) material adheres to the bumps (120) (fig 1). Wherein each array is mounted on a substrate the flux material adheres the bumps to the solder pad openings (242) (fig 2a) (column 5 lines 20-25).

19. Regarding claim 19.

20. Chakravorty teaches prior to mounting each array on a substrate, providing a wafer comprising a plurality of integrated circuit chips (317). Dicing (316) the wafer into of integrated circuit chips comprising two or more integrated circuit chips (9a).

21. Claim 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravorty (US 6181569) in view of Qi (US 6774497) as applied to claim 6 and further in view of Lance (US 5697148)

22. Regarding claim 7

23. Chakravorty in view of Qi teaches elements of the claimed invention above.

24. Chakravorty in view of Qi does not teach cleaning the flux from the device

25. Lance teaches cleaning the flux from the device (column 1 lines 20-35).

26. It would have been obvious to on e of ordinary skill in the art to clean the fluc from the device in order to prevent corrosion.

27. Regarding claim 8

28. Chakravorty in view of Qi teaches elements of the claimed invention above.

29. Chakravorty in view of Qi does not teach injecting the encapsulant.

30. Lance teaches injecting the encapsulant (22) between the chip (12) and the substrate (14).

31. It would have been obvious to one of ordinary skill in the art to inject the encapsulant in order to alleviate problems of thermal mismatch.

32. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravorty (US 6181569) in view of Qi (US 6774497) as applied to claim 5 and further in view of Ho (US 6849955)

33. Regarding claim 9.

34. Chakravorty in view of Qi teaches elements of the claimed invention above.

35. Chakravorty in view of Qi does not teach solder balls formed on the backside of the substrate.

36. Ho teaches forming solder balls (510) formed on the back side of the carrier substrate (100) (fig 8).

37. It would have been obvious to one of ordinary skill in the art to form solder balls on the back side of the carrier substrate in order for the substrate to be electrically connected to a circuit board.

38. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravorty (US 6181569) in view of Qi (US 6774497) as applied to claim 15 and further in view of Lance (US 5697148)

39. Regarding claim 16

40. Chakravorty in view of Qi teaches elements of the claimed invention above.

41. Chakravorty in view of Qi does not teach cleaning the flux from the device

42. Lance teaches cleaning the flux from the device (column 1 lines 20-35).

43. It would have been obvious to on e of ordinary skill in the art to clean the fluc from the device in order to prevent corrosion.

44. Regarding claim 17

45. Chakravorty in view of Qi teaches elements of the claimed invention above.

46. Chakravorty in view of Qi does not teach injecting the encapsulant.

47. Lance teaches injecting the encapsulant (22) between the chip (12) and the substrate (14).

48. It would have been obvious to one of ordinary skill in the art to inject the encapsulant in order to alleviate problems of thermal mismatch.

49. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravorty (US 6181569) in view of Qi (US 6774497) as applied to claim 14 and further in view of Ho (US 6849955)

50. Regarding claim 18.

51. Chakravorty in view of Qi teaches elements of the claimed invention above.

52. Chakravorty in view of Qi does not teach solder balls formed on the backside of the substrate.

53. Ho teaches forming solder balls (510) formed on the back side of the carrier substrate (100) (fig 8).

54. It would have been obvious to one of ordinary skill in the art to form solder balls on the back side of the carrier substrate in order for the substrate to be electrically connected to a circuit board.

Response to Arguments

55. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

56. Applicant's arguments filed 12/10/09 have been fully considered but they are not persuasive.

57. The applicant argues that Chakratvorty does not teach a device comprising a center rows of bumps.

58. As noted in the rejection above Charavorty teaches a device comprising a center row of bumps (fig 7). Central is a broad term which when interpreted broadly, all bumps (311) shown in figure 7 are central. With a narrower interpretation the device comprises central bumps, the inner two columns. With the narrowest interpretation the applicant will note that a row of solder bumps bisects the substrate (302) along the diagonal. The applicant will note that "comprises" does not preclude additional elements and features. MPEP 2111.03.

59. The applicant argues that neither Chakravorty nor Qi address the problem of balancing a center row.

60. In response to applicant's argument that the prior art does not address balancing, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

61. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

62. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID GOODWIN whose telephone number is (571)272-8451. The examiner can normally be reached on Monday through Friday, 9:00am through 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571)272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

djg

/STEVEN LOKE/

Supervisory Patent Examiner, Art Unit 2818